

REMARKS

Prior to the present amendment, claims 1-8 were pending in the present application. Claims 1-3 are amended above. New claims 9-21 are added above. No new matter is added. Entry is respectfully requested.

Applicant notes with appreciation that the Office Action indicates at page 4 that claims 3, 7, and 8 would be allowable if rewritten in independent form. New independent claim 9 includes the limitations of former claims 1 and 3. New dependent claims 10-14 include the limitations of former dependent claims 4-8. New independent claim 15 includes the limitations of former claims 1 and 7. New dependent claims 16-21 include the limitations of former dependent claims 2-6 and 8. Entry and allowance of new independent claims 9 and 15, and new claims 10-14 and 16-21 dependent thereon, are respectfully requested.

Claims 1, 2, and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Roth, *et al.* (U.S. Patent No. 5,118,639 - hereinafter "Roth"). Reconsideration and removal of the rejections are respectfully requested.

In the present invention, as claimed in independent claim 1, a method of fabricating a local interconnection includes forming a "selective epitaxial layer" on "the selective epitaxial growth seed layer pattern," on "a top surface of [a] gate," and on "an exposed surface of the semiconductor substrate." This feature is illustrated at least at FIGs. 3-4 of the present specification. In this example, an epitaxial growth seed layer pattern 140P is formed from an epitaxial growth seed layer 140 such that the pattern remains only in the region of the STI insulating structure (see FIGs. 3-4 and page 6, lines 1-3 of the present specification). A selective epitaxial layer 150 is then formed on the exposed surface of the silicon substrate 100, on the selective epitaxial growth seed layer pattern 140P, and on the gate G (see FIG. 4 and column 6, lines 7-9).

It is submitted that Roth fails to teach or suggest the present invention as claimed in

amended independent claim 1. Specifically, it is submitted that Roth fails to teach or suggest the step of “forming the selective epitaxial layer” on “a top surface of a gate,” as claimed. Instead, in Roth, a seed layer 28 is deposited on isolation region 16, source/drain contact regions 21, 22, and on an encapsulation layer 26 that covers the gate electrode 20 (see Roth, FIG. 3 and column 4, lines 34-37). A photoresist pattern 30 is formed on a portion of the seed layer overlying the isolation region 16 (see Roth, FIG. 3 and column 4, lines 51-53). The seed layer 28 is etched using the photoresist pattern as a mask, and the photoresist pattern 30 is removed to expose a nucleation pattern 32 formed from the seed layer 28 (see Roth, FIG. 4 and column 4, lines 61-64). Epitaxial silicon is selectively grown on the nucleation pattern 32 and on the exposed source/drain contact regions 21, 22 (see Roth, FIG. 5 and column 5, lines 44-47) to form source and drain lead extensions 38, 40, which are coextensive with the nucleation pattern 32 (see Roth, FIG. 5 and column 5, lines 51-55). No epitaxial silicon growth occurs on the Roth gate electrode 20 because of the presence of the insulative encapsulation layer 26.

In view of the above, it is submitted that Roth fails to teach or suggest the invention set forth in amended independent claim 1. In particular, Roth fails to teach or suggest “forming the selective epitaxial layer...on a top surface of the gate,” as claimed in amended independent claim 1. Removal of the rejections and allowance of independent claim 1 are therefore respectfully requested. With regard to dependent claims 2 and 4-6, it follows that these claims should inherit the allowability of independent claim 1 from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Mills & Onello, LLP  
Eleven Beacon Street, Suite 605  
Boston, MA 02108  
Telephone: (617) 994-4900, Ext. 4902  
Facsimile: (617) 742-7774  
J:\SAM\0539\amenda\amendmenta.wpd

Anthony P. Onello  
Anthony P. Onello, Jr.  
Registration Number 38,572  
Attorney for Applicant